Claims:

1. A storage device, comprising:

a cache array having cache lines filled with contiguous instructions in an instruction cache (ICache) portion that is adjacent to a trace cache (TCache) portion where cache lines are filled with elements of a trace.

2. The storage device of claim 1 further including an indexing logic where the ICache portion is looked-up when the TCache portion is not supplying instructions.

3. The storage device of claim 1 wherein neither the ICache portion nor the TCache portion is looked-up when the TCache portion is supplying instructions.

4. The storage device of claim 1 wherein a line in the TCache portion is indexed when a branch instruction is executed.

5. The storage device of claim 1 wherein the TCache portion contains non-contiguous instructions from an instruction stream.

6. A system, comprising:

a processor;

first and second antennas to receive modulated signals and supply a signal to the processor; and

a cache having in one array both an instruction cache (ICache) portion and a trace cache (TCache) portion, where a line in the TCache portion is indexed when the processor takes a branch.

7. The system of claim 6 wherein the TCache portion is further indexed when the processor takes a jump, a call or a return.

8. The system of claim 6 further including an indexing logic where the ICache portion is looked-up when the TCache portion is not supplying instructions.

9. The system of claim 8 wherein the indexing logic is not used for either the ICache portion or TCache portion when the TCache portion is supplying instructions.

10. A method, comprising:

intermingling cache lines in one array of a cache where a first cache line in a trace cache (TCache) portion is physically adjacent a second cache line in an instruction cache (ICache) portion.

11. The method of claim 10, further including:

dynamically changing a number of lines in the ICache portion and the TCache portion.

12. The method of claim 10, further including:

dynamically altering a size of the ICache portion and the TCache portion in the one array as time progresses.

13. The computer system of claim 10, further including:

supplying a program-order stream of instructions from each cache line in the TCache portion.

14. The computer system of claim 10, further including:

supplying instructions in program order from cache lines in the ICache portion until a branch is encountered.

15. The computer system of claim 10, further including:

associating a next address with the first cache line in the TCache portion to allow a next line to be ready before a current line is completely fetched.

16. A method comprising:

using one control circuit to fill an array with instruction cache (ICache) cache lines mixed with trace cache (TCache) cache lines where an allocated proportion of ICache cache lines to TCache cache lines is dynamically changing with time.

17. The method of claim 16, comprising:

using an address of a next instruction when an end of a cache line is reached to determine use of the ICache cache lines or the TCache cache lines.

18. The method of claim 16, comprising:

searching both the ICache cache lines and the TCache cache lines when an address is a result of a branch target.

19. The method of claim 16, comprising:

using the TCache cache lines when an address is found in the TCache cache lines.

20. The method of claim 19, comprising:

using the ICache cache lines when the address is found in the ICache cache lines and not in the TCache cache lines.